UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,011	12/13/2001	Laurent A. Six	TI-29536	2461

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EXAMINER
TABONE JR, JOHN J

ART UNIT	PAPER NUMBER
2133	4

DATE MAILED: 05/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2001*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
   closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *12/31/01* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All   b)☐ Some * c)☐ None of:

   1.☐ Certified copies of the priority documents have been received.

   2.☐ Certified copies of the priority documents have been received in Application No. _____.

   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
      application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)   4)☐ Interview Summary (PTO-413)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)   Paper No(s)/Mail Date. _____ .
3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)   5)☐ Notice of Informal Patent Application (PTO-152)
   Paper No(s)/Mail Date *3*.   6)☐ Other: _____ .

DETAILED ACTION

1.   Claims 1-20 have been examined. Preliminary amendment dated 12/13/2001 has

been entered.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2.   Claims 3, 4, 10, 11, 19 and 20 are rejected under 35 U.S.C. 112, first paragraph,

as failing to comply with the enablement requirement. The claim(s) contains subject

matter which was not described in the specification in such a way as to enable one

skilled in the art to which it pertains, or with which it is most nearly connected, to make

and/or use the invention.

Claims 3, 10, and19:

"**and to receive functional data over the test line and the functional clock

signal while the device is in the switch mode.**"

The switch mode portion of this claim is not enabled by the specification

disclosed on page 13, lines 21-29 and page 14 lines 1 and 2. According to the

disclosure on these pages the device receives test data from the TD line 52 in Fig. 2

NOT functional data, which is line 50. Also, the specification describes the "test line" as

test line 56 (page 13, line 26). This is not a data line, but an input to the OR gate 68.

The device cannot receive data over the test line as written. Correction is required.

<u>Claims 4, 11 and 20:</u>

These claims are rejected because they depend on rejected base claims 3, 10

and 19, respectively and contain the same problems of enablement. In addition,

because of the ambiguity of the base claims 3, 10 and 19 these claims are not rejected

over prior art.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3.   Claims 1, 2, 5-9, and 12-18 are rejected under 35 U.S.C. 102(e) as being

anticipated by Kurtulik et al. (US2002/0125907).

<u>Claims 1, 9, and 16:</u>

Kurtulik teaches in Fig. 6 the ABIST engine 602 (state machine) generates word

addresses, bit addresses, data-in, clocks and controls 604, as a serial stream of bits

and shifts the data to the appropriate arrays 612 (device memory) via the <u>scan chain</u>

610. (Page 4, ¶ 41).

"a state machine operable to divide the scan chain into a plurality of sub-

chains,"

Kurtulik teaches the scan chain 610 is reconfigured during scan ABIST mode to a
shorter array sub-chain. (Page 4, ¶ 41).

"to provide a first data set in the sub-chains,"

Kurtulik teaches ABIST engine 602 (state machine) generates data-in as a serial
stream of bits and shifts the data to the appropriate arrays 612 (device memory) <u>via the
scan chain</u> 610. (Page 4, ¶ 41).

"to link the sub-chains in parallel,"

Kurtulik teaches the scan chain 704 is configured as a number of parallel sub-
chains. (Page 4, ¶ 43).

"to link the sub-chains to the device memory,"

Kurtulik teaches the ABIST engine 602 (state machine) generates word
addresses, bit addresses, data-in, clocks and controls 604, as a serial stream of bits
and shifts the data to the appropriate arrays 612 (device memory) via the <u>scan chain</u>
610. Kurtulik also teaches the ABIST engine 602 (state machine) writes and reads data
from the array 612 (linking sub-chains to the write port and read port of the memory
device, from claim 9). (Page 4, ¶ 41).

**"to execute a first application to update the first data set in the sub-chains,
the first application operable to use the channel,"**

Kurtulik teaches various algorithms programmed into the ABIST engine can
supply different data-in patterns and address stepping to the array 612. (Page 4, ¶ 41).

"to shift the updated first data set into the device memory for storage,"

Kurtulik teaches a single operation performed on all arrays, for example a write,

requires that the entire sub-chain be scanned with the address and data-in patterns for

each array 612. (Page 4, ¶ 41).

"to shift a second data set from the device memory into the sub-chains,

and to execute a second application to update the second data set in the sub-

chains, the second application operable to use the channel."

Kurtulik teaches the controls and write clock 604 are activated once the scan in

606 address and data are set up, and all arrays 612 are written simultaneously. Kurtulik

further teaches that the entire sub-chain is then reloaded serially (second data set) by

the ABIST engine 602 to set up for the next array operation. (Page 4, ¶ 41).

Claim 2:

Kurtulik teaches a write operation performed on all arrays requires that the entire

sub-chain be scanned with the address and data-in patterns for each array 612 (shifting

through the writer port). Kurtulik teaches the data-out register from each array 612 (read

port) feeds a dedicated MISR 618 forming an accumulated signature representing the

compressed output data from that array 612. The MISR 618 for each array 612 (device

memory) are in the ABIST sub-chain. (Page 4, ¶ 41 and 42).

Claims 5 and 12:

These claims are rejected per claims 1, 9, and 16. Kurtulik teaches various

algorithms programmed into the ABIST engine (state machine) can supply different

data-in patterns and address stepping to the array 612 (storing/shifting third and fourth

data set). Kurtulik also teaches the ABIST engine 602 reloads the array for the next

operation (restoring/shifting third and fourth data set). (Page 4, ¶ 41 and 42).

Claims 6 and 13:

Kurtulik teaches the present invention is a method for testing semiconductor

integrated circuits (ASIC, FPGA). (Page 1, ¶ 2 and 12).

Claims 7, 14 and 17:

Kurtulik teaches the ABIST engine 602 generates word addresses, bit

addresses, data-in, clocks and controls 604, as a serial stream of bits and shifts the

data to the appropriate arrays via the scan chain. Scan chains inherently include flip-

flops as the clocked sequential elements in the chain or sub-chains. (Page 4, ¶ 41).

Claims 8, 15 and 18:

Kurtulik teaches the ABIST engine 602 (state machine) generates word

addresses, bit addresses, data-in, clocks and controls 604, as a serial stream of bits

and shifts the data to the appropriate arrays 612 (device memory) via the scan chain

610. Kurtulik further teaches the scan chain 610 is reconfigured during scan ABIST

mode to a shorter array sub-chain with only the necessary data and address bits

(specified number of sub-chains correspond to the data width of the device memory) to

be scanned in 606 for each array sub-chain. (Page 4, ¶ 41).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4.   Claims 3, 10, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Kurtulik et al. (US2002/0125907) in view of Rearick (US 6715105).

Claims 3, 10, and 19:

Kurtulik does not explicitly teach "a switch mode for switching between applications",

however, Kurtulik does teach the ABIST engine 602 (state machine) generates word

addresses, bit addresses, data-in, clocks (test and functional) and controls 604, as a

serial stream of bits and the scan chain 610 is reconfigured during scan ABIST mode

(test mode). (Page 4, ¶ 41). Rearick teaches data (test data) is scanned into one or

more scanpaths 172 from a scan data in (SDI) port 122 (test line) under the control of a

scan clock signal SCAN_CLK 126 (test clock), either directly or indirectly through a

linear feedback shift register (LFSR) 102. Rearick further teaches the system execution

clock CLK 109 (functional clock) is used to capture normal system data (functional data)

into the registers comprising the scan path. (Col. 5, lines 60-67; col. 6, lines 1-6).

Rearick also suggests the state of the TAP controller 130 is controlled by a test clock

and a test mode select signal (switch mode). Rearick discloses that during normal

operation of the host (functional mode), the TAP is forced into the Test-Logic-Reset

state by driving the test mode select signal high and applying six or more test clock

pulses. In this state, Rearick explains, the TAP issues a reset signal that places all test

logic in a condition that does not impeded normal operation of the host (receives

functional data over a test line while in switch mode). (Col. 8, lines 1-16). It would have

been obvious to one of ordinary skill in the art at the time the invention was made to

modify Kurtulik's ABIST engine 602 (state machine) with Rearick's TAP controller 130

(also a state machine) to include Rearick's test mode select signal (switch mode) in the

generatation of Kurtulik's clocks (test and functional) and controls 604. The artisan

would be motivated to do so because this would enable Kurtulik's ABIST engine 602 to

switch modes of applications between test and functional mode in loading data into the

memory array 612.

Conclusion

The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.
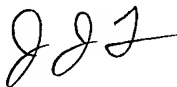
Bhawmik (US-6370664)

Bhawmik teaches test system for testing an integrated circuit which includes a

plurality of flip-flops arranged in a scan chain, a memory register for storing random test

vectors (data). Bhawmik also teaches a plurality of parallel scan chains depending on

the specific function. This pertain to claims 1, 9, and 16, 3,10, and 19, 6 and 13, 7, 14,

and 17 and 8.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to John J Tabone, Jr. whose telephone number is (703)

305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JJT

Albert DeCady
Primary Examiner